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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/764,208	01/19/2001	Jae-Choon Lee	0630-1210P	7426

2292 7590 05/22/2002

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EXAMINER

LEVI, DAMEON E

ART UNIT PAPER NUMBER

2841

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/764,208

Applicant(s)

HWANG ET AL.

Examiner

Dameon E Levi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/20/2002 Amendment Paper No. 4.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01-19-01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Lu et al US Patent 5933343.

Regarding claim 1, the admitted prior art discloses:

- a one system module in which a socket is placed between a ceramic PCB and an epoxy PCB that are disposed inside a module body (see elements 13,11,12, Fig 1)
- a power element and signal elements are respectively mounted on the upper portion of each PCB (see Fig 1, page 1, lines 24-25, page 2, lines 21-22)
- a groove is made at the lower side surface and at the middle side surface of the module body to support the ceramic PCB and the epoxy PCB to form a two-story structure (see Fig 1)
- a power pin for receiving a power signal from an external source is mounted on the upper portion of at least one edge of the ceramic PCB (see page 3, line 12, see Fig 1)

The admitted prior art does not disclose a signal pin for receiving various signals from an external source is mounted on the upper portion of at least one edge of the epoxy PCB in line with the power pin.

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Lu et al discloses a module disclosing a signal pin for receiving various signals from an external source is mounted on the upper portion of at least one edge of an epoxy PCB in line with a power pin (see elements 24,32 Figs 2,3, column 3,lines 28-36).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted the power and signal pins upon the ceramic and epoxy PCBs respectively as disclosed by Lu et al in the prior art device for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective circuits and the corresponding external devices or circuits to which they are connected.

Regarding claim 2, the admitted prior art discloses wherein aluminum wire bonding is performed to mount elements on the ceramic PCB, while gold wire bonding is performed to mount a microcomputer on the epoxy PCB (see page 3, lines 8-11).

Also regarding claim 2, the limitation [wherein aluminum wire bonding is performed to mount elements on the ceramic PCB, while gold wire bonding is performed to mount a microcomputer on the epoxy PCB] are process limitations in a product claim and cannot serve to patentably define the product over the prior art of record [Lu et al, admitted prior art]; [see Product –by-process, MPEP 2113 and 2173.05(p)]

It is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product.(In re Johnson, 157 USPQ 670, 1968).

Regarding claim 3 the mounting of power and signal pins to PCBs by the technique of soldering is conventional in the art(Lu et al column 3, lines25-26, 34-34).

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Additionally regarding claim 3, the limitation [..wherein the power pin is mounted on the ceramic PCB by soldering, while the signal pin is mounted on the epoxy PCB by soldering] is a process limitation in a product claim and cannot serve to patentably define the product over the prior art of record []; [see Product –by-process, MPEP 2113 and 2173.05(p)]

It is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art , cannot impart patentability to that product.(In re Johnson, 157 USPQ 670, 1968).

Regarding claim 5, the admitted prior art discloses the instant claimed invention except wherein power pins are mounted on the upper portion of both edges of the ceramic PCB and signal pins are mounted on the upper portion of both edges of the epoxy PCB in line with the power pins.

Lu et al discloses a module disclosing wherein power pins are mounted on the upper portion of both edges of a PCB and signal pins are mounted on the upper portion of both edges of an epoxy PCB in line with the power pins (see elements 24,32 Figs 2,3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted the power and signal pins upon the ceramic and epoxy PCBs respectively in line on both edges of the PCB's as disclosed by Lu et al in the prior art device for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective circuits and the corresponding external devices or circuits to which they are connected.

Regarding claim 6, the admitted prior art discloses a one system module comprising:

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- a module body, the module body including an inside surface having a first groove formed at a lower portion thereof and a second groove formed at a mid portion thereof; a ceramic printed circuit board (PCB) supported in the first groove so as to be disposed inside the module body, the ceramic PCB having power elements secured thereto an epoxy PCB supported in the second groove so as to be disposed inside the module body, the epoxy PCB having signal elements secured thereto (see element 11,12, see grooves in element 10 Fig 1)
- a socket located between the ceramic PCB and the epoxy PCB, the socket establishing electrical communications between the power elements of the ceramic PCB and the signal elements of the epoxy PCB (see element 13, Fig 1)
- a power pin mounted on an upper surface and along a first edge of the ceramic PCB, the power pin for receiving a power signal from a source external to the module body (see page 3,line 12, see Fig 1)

The admitted prior art does not disclose a signal pin mounted on an upper surface and along a first edge of the epoxy PCB, the signal pin for receiving various signals from a source external to the module body, wherein the signal pin is linearly arranged relative to the power pin.

Lu et al discloses a module disclosing a signal pin mounted on an upper surface and along a first edge of an epoxy PCB, the signal pin for receiving various signals from a source external to the module body, wherein the signal pin is linearly arranged relative to a power pin.

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Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted the power and signal pins upon the ceramic and epoxy PCBs respectively in the manner as disclosed by Lu et al in the prior art device for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective circuits and the corresponding external devices or circuits to which they are connected.

Regarding claim 7, the admitted prior art discloses the instant claimed invention except further comprising:

a second power pin mounted on the upper surface and along a second edge of the ceramic PCB, wherein the second edge of the ceramic PCB is opposite the first edge of the ceramic PCB; and a second signal pin mounted on the upper surface and along a second edge of the epoxy PCB, wherein the second edge of the epoxy PCB is opposite the first edge of the epoxy PCB.

Lu et al discloses a module comprising a second power pin mounted on an upper surface and along a second edge of a ceramic PCB, wherein the second edge of the ceramic PCB is opposite the first edge of the ceramic PCB; and a second signal pin mounted on an upper surface and along a second edge of an epoxy PCB, wherein the second edge of the epoxy PCB is opposite the first edge of the epoxy PCB (see elements 24,32 Figs 2,3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted the power and signal pins upon the ceramic and epoxy PCBs respectively in the manner as disclosed by Lu et al in the prior art device

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for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective circuits and the corresponding external devices or circuits to which they are connected.

Regarding claim 8, the admitted prior art discloses the instant claimed invention except wherein the second signal pin is linearly arranged relative to the second power pin.

Lu et al discloses a module wherein second signal pin is linearly arranged relative to a second power pin.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have arranged the power and signal pins respectively in the manner as disclosed by Lu et al in the prior art device for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective circuits and the corresponding external devices or circuits to which they are connected.

Regarding claim 9, the admitted prior art discloses wherein the signal elements include a microprocessor (see Fig 1, see page 2, lines 2-3, 21-22).

Regarding claims 10-12, the techniques of gold wire bonding, aluminum wire bonding, and soldering are conventional in the art(see page 3, lines 8-11, see Lu et al column 3, lines 25-26, 34-34).

Response to Arguments

Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

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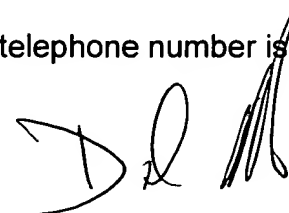
Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E Levi whose telephone number is (703) 305-0426. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David S Martin can be reached on (703) 308-3121. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0058.



DAVID MARTIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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Dameon E Levi
Examiner
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May 9, 2002